ICFPT 2013 Technical program

[Design Competition] (8 December 2013)

9:00	12:00	**Pre-competition check**
13:00	17:00	**Pre-finals**

[ICFPT2013 Program] Day 1 (9 December 2013)

8:50	9:00	**Opening**
		Keynote Lecture I Session Chair: Hideharu Amano (Keio University)
9:00	10:00	Recent Advances in Die Stacking and 3D FPGA Dr. Arif Rahman Altera Corp.
		Poster Session I
10:00	11:00	(poster presentation)
		1.1 Best Paper Candidate Session Session Chair: Yoshiki Yamaguchi (University of Tsukuba)
11:00	11:20	Accelerating Validation of Time-Triggered Automotive Systems on FPGAs Shreejith Shanker, Suhaib Fahmy and Martin Lukasiewycz
11:20	11:40	Exploiting Partially Defective LUTs: Why You Don't Need Perfect Fabrication André DeHon and Nikil Mehta
11:40	12:00	Maximum Flow Algorithms for Maximum Observability During FPGA Debug Eddie Hung, Al-Shahna Jamal and Steven J.E. Wilton
12:00	12:20	The Architecture and Placement Algorithm for A Uni-Directional Routing Based 3D FPGA Junsong Hou, Heng Yu, Yajun Ha and Xin Liu
12:20	14:00	**Solarflare Luncheon Session (Sponsored Session)** Session Chair: Kentaro Sano (Tohoku University)
		1.2 Architecture Session Chair: Guy Lemieux (University of British Columbia)
14:00	14:20	COFFE: Fully-Automated Transistor Sizing for FPGAs Charles Chiasson and Vaughn Betz
14:20	14:40	A Case for Hardened Multiplexers in FPGAs S. Alexander Chin and Jason H. Anderson
14:40	15:00	Debugging Processors with Advanced Features by Reprogramming LUTs on FPGA Satoshi Jo, Amir Masoud Gharehbaghi, Takeshi Matsumoto and Masahiro Fujita
15:00	15:20	**Break**
		1.3 FPGA Appliactions I Session Chair: Andre DeHon (University of Pennsylvania)
15:20	15:40	Virtual-to-Physical Address Translation for an FPGA-based Interconnect with Host and GPU Remote DMA Capabilities. Roberto Ammendola, Andrea Biagioni, Ottorino Frezza, Francesca Lo Cicero, Alessandro Lonardo, Pier Stanislao Paolucci, Davide Rossetti, Francesco Simula, Laura Tosoratto and Piero Vicini
15:40	16:00	Accelerating Iterative Algorithms with Asynchronous Accumulative Updates on FPGAs Deepak Unnikrishnan, Sandesh Virupaksha, Lekshmi Krishnan, Lixin Gao and Russell Tessier
16:00	16:20	High Throughput, Tree Automata based XML Processing using FPGAs Reetinder Sidhu
16:20	16:40	Transparent FPGA based Device for SQL DDoS Mitigation Karthikeyan Pandiyarajan, Srijith Haridas and Kuruvilla Varghese
16:40	17:00	**Break**
		1.4 Power-Aware and Dynamically Reconfigurable Systems Session Chair: Jason Anderson (University of Toronto)
17:00	17:20	Discrete Event System Specification, Synthesis, and Optimization of Low-Power FPGA-based Embedded Systems Tim Pifer, David Schwartz, Roman Lysecky, Chungman Seo and Bernard Zeigler
17:20	17:40	Optimizing Time and Space Multiplexed Computation in a Dynamically Reconfigurable Processor Takao Toi, Noritsugu Nakamura, Taro Fujii, Toshio Kitaoka, Katsumi Togawa, Koichiro Furuta and Toru Awashima
18:00	20:00	**Welcome Reception**
18:00	20:00	**Demo / Ph.D Forum / Design Competition Posters**

[ICFPT2013 Program] Day 2 (10 December 2013)

8:30	8:40	**Announcement**
		Keynote Lecture II Session Chair: Kazutoshi Kobayashi(Kyoto Institute of Technology)
8:40	9:40	Reconfigurable chip Advantage compared with GPGPU from the compiler perspective Dr. Kazutoshi Wakabayashi NEC Corp.
		Poster Session II
9:40	10:40	(poster presentation)
		2.1 High Level Synthesis I Session Chair: Qiang Liu (Tianjin University)
10:40	11:00	SOAP: Structural Optimization of Arithmetic Expressions for High-Level Synthesis Xitong Gao, Samuel Bayliss and George Constantinides
11:00	11:20	Making Domain-Specific Hardware Synthesis Tools Cost-Efficient Nithin George, David Novo, Tiark Rompf, Martin Odersky and Paolo Ienne
11:20	11:40	System-Level FPGA Device Driver with High-Level Synthesis Support Vipin Kizhepatt, Shreejith Shanker, Dulitha Gunasekara, Suhaib Fahmy and Nachiket Kapre
11:40	12:00	Bitwidth-Optimized Hardware Accelerators with Software Fallback Ana Klimovic and Jason Anderson
12:00	13:30	**Lunch**
		2.2 FPGA Applications II Session Chair: Tsutomu Maruyama (University of Tsukuba)
13:30	13:50	Implementation of High Performance Hardware Architecture of OpenSURF Algorithm on FPGA Xitian Fan, Chenlu Wu, Wei Cao, Xuegong Zhou, Shengye Wang and Lingli Wang
13:50	14:10	TROJANUS: An Ultra-Lightweight Side-Channel Leakage Generator for FPGAs Sebastian Kutzner, Axel Poschmann and Marc Stöttinger
14:10	14:30	Real-time and Low Power Embedded L1-Optimization Solver Design Zhi Ping Ang and Akash Kumar
14:30	14:50	A Low Latency Kernel Recursive Least Squares Processor using FPGA Technology Yeyong Pang, Shaojun Wang, Yu Peng, Nick Fraser and Philip H.W. Leong
14:50	15:10	**Break**
		2.3 (Special Session) Coarse Grain Reconfigurable Architectures for Graphics Session Chairs: Soojung Ryu (SAMSUNG Electronics) and Steve Wilton (University of British Columbia)
15:10	15:30	Efficient Execution of Augmented Reality Applications on Mobile Programmable Accelerators Jason Jong Kyu Park, Yongjun Park and Scott Mahlke
15:30	15:50	An OpenCL Optimizing Compiler for Reconfigurable Processors Jeongho Nah, Jun Lee, Hongjune Kim, Jinseok Lee, Seok Joong Hwang, Donghoon Yoo and Jaejin Lee
15:50	16:10	Real-time Ray Tracing on Coarse-grained Reconfigurable Processor Jaedon Lee, Youngsam Shin, Won-Jong Lee, Soojung Ryu and Jeongwook Kim
16:10	16:30	Mobile GPU Shader Processor based on Non-blocking Coarse Grained Reconfigurable Arrays Architecture Kwontaek Kwon, Sungjin Son, Jeongsoo Park, Jeongae Park, Sangoak Woo, Seokyoon Jung and Soojung Ryu
16:30	21:30	**Banquet**

ICFPT 2013 Technical program

[ICFPT2013 Program] Day 3 (11 December 2013)

8:30	8:40	**Announcement**
		Keynote Lecture III Session Chair: Yajun Ha (National University of Singapore)
8:40	9:40	Why Put FPGAs in Your CPU Socket? Prof. Paul Chow Univ. of Toronto
		Poster Session III
9:40	10:40	(poster presentation)
		3.1 High Performance Computing Session Chair: Dirk Koch (University of Manchester)
10:40	11:00	Acceleration of Real-time Proximity Query for Dynamic Active Constraints Thomas C.P. Chau, Ka-Wai Kwok, Gary C.T. Chow, Kuen Hung Tsoi, Kit-Hang Lee, Zion Tse, Peter Y.K. Cheung and Wayne Luk
11:00	11:20	Dynamic Stencil: Effective Exploitation of Run-time Resources in Reconfigurable Clusters Xinyu Niu , Jose G. F. Coutinho , Yu Wang and Wayne Luk
11:20	11:40	FlexGrip: A Soft GPGPU for FPGAs Kevin Andryc, Murtaza Merchant and Russell Tessier

0:00	1:30	**Lunch**
		3.2 Physical Level EDA Session Chair: Vaughn Betz (University of Toronto)
1:30	1:50	Maximizing Speed and Density of Tiled FPGA Overlays via Partitioning Charles Eric LaForest and J. Gregory Steffan
1:50	2:10	Improving Clock-Rate of Hard-Macro Designs Christopher Lavin, Brent Nelson and Brad Hutchings
2:10	2:30	Exploiting Stochastic Delay Variability on FPGAs with Adaptive Partial Rerouting Zhenyu Guan, Justin S. J. Wong, Sumanta Chaudhuri, George Constantinides and Peter Y. K. Cheung
2:30	2:50	Automated Multi-Device Placement, I/O Voltage Supply Assignment, and Pin Assignment in Circuit Board Design Daniel Seemuth and Katherine Morrow
2:50	3:10	**Break**
		3.3 High Level Synthesis II Session Chair: Christian Plessl (University of Paderborn)
3:10	3:30	From Software Threads to Parallel Hardware in High-Level Synthesis for FPGAs Jongsok Choi, Stephen Brown and Jason Anderson
3:30	3:50	StML: Bridging the Gap between FPGA Design and HDL Circuit Description Dustin Peterson, Oliver Bringmann, Thomas Schweizer and Wolfgang Rosenstiel
3:50	4:10	Derivation of Efficient FSM from Loop Nests Tomofumi Yuki, Antoine Morvan and Steven Derrien
4:10	4:30	An Automated Flow for the High Level Synthesis of Coarse Grained Parallel Applications Vito Giovanni Castellana and Fabrizio Ferrandi
4:30	4:40	**Closing**
4:40	6:40	**Design Competition (Final)**

[Workshop] (12 December 2013)

9:30	16:30	**Xilinx Workshop "System Design Flow using Vivado"**
13:00	17:00	**Cypress Workshop "PSoCTM4 Workshop"**

[Workshop] (13 December 2013)

9:30	16:30	**Xilinx Workshop "System Design Flow using Vivado"**

Poster Session I (DAY1: 9 December 10:00-11:00)

A High-Throughput FPGA Architecture for Parallel Connected Components Analysis Based on Label Reuse
Michael Klaiber, Donald Bailey, Silvia Ahmed, Yousef Baroud and Sven Simon

Teaching FPGA Security
Lilian Bossuet

Fast Boolean Matching Based on NPN Classification
Zheng Huang, Lingli Wang, Yakov Nasikovskiy and Alan Mishchenko

Multi-Personality Partitioning for Heterogeneous Systems
Anthony Gregerson, Aman Chadha and Katherine Morrow

A Hardware Acceleration of a Phylogenetic Tree Reconstruction with Maximum Parsimony Algorithm using FPGA
Henry Block and Tsutomu Maruyama

Application-Specific Customisation of Market Data Feed Arbitration
Stewart Denholm, Hiroaki Inoue, Takashi Takenaka and Wayne Luk

A Connection-based Router for FPGAs
Elias Vansteenkiste, Karel Bruneel and Dirk Stroobandt

Flexible Hierarchy Ray Tracing on FPGAs
Sam Collinson and Oliver Sinnen

Design and Optimization of Heterogeneous Tree-based FPGA using 3D Technology
Vinod Pangracious, Zied Marrakchi and Habib Mehrez

NFA Reduction for Regular Expressions Matching Using FPGA
Vlastimil Košař, Martin Žádník and Jan Kořenek

Runtime Hardware/Software Task Transition Scheduling for Runtime-Adaptable Embedded Systems
Nathan Sandoval, Casey Mackin, Sean Whitsitt, Roman Lysecky and Jonathan Sprinkle

A Speculative Gather System for Cool Mega-Array
Rie Uno, Nobuaki Ozaki, Mai Izawa, Akihito Tsusaka, Takaaki Miyajima and Hideharu Amano

Poster Session II (DAY2: 10 December 9:40-10:40)

An Acceleration Method of Short Read mapping using FPGA
Yoko Sogabe and Tsutomu Maruyama

Quantum FPGA Architecture Design
Jialin Chen, Lingli Wang and Bin Wang

Real-time High-quality Stereo Vision System in FPGA
Wen-Qiang Wang, Jing Yan, Ning-Yi Xu, Yu Wang and Feng-Hsiung Hsu

High-Level Synthesis of Dynamic Data Structures: A Case Study Using Vivado HLS
Felix Winterstein, Samuel Bayliss and George Constantinides

Datapath Fault Tolerance for Parallel Accelerators
James J. Davis and Peter Y. K. Cheung

Hardware Acceleration of Biomedical Models with OpenCMISS and CellML
Ting Yu, Chris Bradley and Oliver Sinnen

sAES A High Throughput and Low Latency Secure Cloud Storage with Pipelined DMA Based PCIe Interface
Yongzhen Chen, Miguel Rodel Felipe, Yi Wang, Yajun Ha, Shuqin Ren and Khin Mi Mi Aung

A 66.1 Gbps Single-pipeline AES on FPGA
Qiang Liu, Zhenyu Xu and Ye Yuan

Partially Reconfigurable Flux Calculation Scheme in Advection Term Computation
Mohamad Sofian Abu Talip, Takayuki Akamine, Mao Hatto, Yasunori Osana, Naoyuki Fujita and Hideharu Amano

FPGA-accelerated Key Search for Cold-Boot Attacks against AES
Heinrich Riebler, Tobias Kenter, Christoph Sorge and Christian Plessl

A Low power Reconfigurable Accelerator using a Back-gate Bias Control Technique
Hongliang Su, Weihan Wang, Kuniaki Kitamori and Hideharu Amano

Adaptive Compression for Instruction Code of Coarse Grained Reconfigurable Architectures
Moo-Kyoung Chung, Jun-Kyoung Kim, Yeon-Gon Cho and Soojung Ryu

Poster Session III (DAY3: 11 Deccember 9:40-10:40)

High-order Reconfigurable FIR Filter Design Based on Statistical Analysis of CSD Coefficients
Rui Jia, Fei Wang, Rui Chen, Xin-Gang Wang, Delong Shang and Hai-Gang Yang

Color configuration method for an optically reconfigurable gate array
Takumi Fujimori and Minoru Watanabe

Revisiting the reduction circuit: a case study for simultaneous architecture and precision optimisation
David Boland and George A. Constantinides

EasyPR - an Easy Usable Open Source PR System
Dirk Koch, Christian Beckhoff, Alexander Wold and Jim Torresen

A Hardware Implementation of Bag of Words and Simhash for Image Recognition
Shengye Wang, Chen Liang, Xuegong Zhou, Wei Cao, Chenlu Wu, Xitian Fan and Lingli Wang

An FPGA-cluster-accelerated Match Engine for Content-based Image Retrieval
Chen Liang, Chenlu Wu, Xuegong Zhou, Wei Cao, Shengye Wang and Lingli Wang

Spatio-Temporally-Shared Reconfigurable Fast Fourier Transform Architecture Design
Hung-Lin Chao, Chun-Yang Peng, Cheng-Chien Wu, Ken-Shin Huang, Chun-Hsien Lu, Jih-Sheng Shen and Pao-Ann Hsiung

A high-speed FFT based on a six-step algorithm: Applied to a radio telescope for a solar radio burst
Hiroki Nakahara, Kazumasa Iwai and Hiroyuki Nakanishi

A Defect-tolerant Cluster in a Mesh SRAM-based FPGA
Arwa Ben Dhia, Rehman Saif Ur, Adrien Blanchardon, Lirida Naviner, Mounir Benabdenbi, Roselyne Chotin-Avot, Emna Amouri, Habib Mehrez and Zied Marrakchi

Reconfigurable Filtered Acceleration of Short Read Alignment
James Arram, Wayne Luk and Peiyong Jiang

Efficient methods for out-of-order load/store execution for high-performance soft processors
Henry Wong, Vaughn Betz and Jonathan Rose

Semantics-directed Machine Architecture in ReWire
Adam Procter, William Harrison, Ian Graves, Michela Becchi and Gerard Allwein

ZCluster: A Zynq-based Hadoop Cluster
Zhongduo Lin and Paul Chow

A Non-intrusive Portable Fault Injection Framework to Assess Reliability of FPGA-based Designs
Elyas Abolhassani Ghazaani, Zana Ghaderi and Seyed Ghassem Miremadi

Demo / Ph.D Forum / Design Competition Posters (DAY1: 9 December 18:00-20:00)
Demo
An Open-Source SATA Core for Virtex-4 FPGAs Cory Gorman, Paul Siqueira, and Russell Tessier
Direct Virtual Memory Access from FPGA for High-Productivity Heterogeneous Computing Ho-Cheung Ng, Yuk-Ming Choi and Hayden Kwok-Hay So
Testing Reliability Techniques for SoCs with Fault Tolerant CGRA by using live FPGA Fault Injection Johannes Maximilian Kühn, Thomas Schweizer, Dustin Peterson, Tommy Kuhn and Wolfgang Rosenstiel
Task level pipelining with PEACH2: an FPGA switching fabric for high performance computing Takaaki Miyajima, Takuya Kuhara, Toshihiro Hanawa, Hideharu Amano and Taisuke Boku
Enhancing Communication On Automotive Networks Using Data Layer Extensions Shreejith Shanker and Suhaib A. Fahmy
A Prototyping System for Hardware Distributed Objects with Diversity of Programming Languages Takeshi Ohkawa, Takashi Yokota and Kanemitsu Ootsu
Ph.D Forum
Fast Simulation of Digital Spiking Silicon Neuron Model Employing Reconfigurable Dataflow Computing Will Li, Shridhar Chaudhary, Ray Cheung, Takeshi Matsumoto and Masahiro Fujita
Hardware acceleration for the banded Smith-Waterman algorithm with the cycled systolic array Peng Chen, Chao Wang, Xi Li and Xuehai Zhou
Design Competition
Implementation of a Highly Scalable Blokus Duo Solver on FPGA Chester Liu
From C to Blokus Duo with LegUp High-Level Synthesis Jiu Cheng Cai, Mengyao Wang, Ruolong Lian, Andrew Canis, Jongsok Choi, Blair Fort, Emily Miao, Yanyan Zhang, Nazanin Calagar, Stephen Brown and Jason Anderson
The Liquid Metal Blokus Duo Design Erik Altman, Joshua Auerbach, David Bacon, Ioana Baldini, Perry Cheng, Stephen Fink, Rodric Rabbah and Sunil Shukla
FPGA Blokus Duo Solver using a massively parallel architecture Takashi Yoza, Retsu Moriwaki, Yuki Torigai, Yuki Kamikubo, Takayuki Kubota, Takahiro Watanabe, Takumi Fujimori, Hiroyuki Ito, Masato Seo, Kouta Akagi, Yuichiro Yamaji and Minoru Watanabe
Artificial Intelligence of Blokus Duo on FPGA Using Cyber Work Bench Naru Sugimoto, Takaaki Miyajima, Takuya Kuhara, Yuki Katuta, Takushi Mitsuichi and Hideharu Amano
An FPGA-based specific processor for Blokus Duo Javier Olivito, Javier Resano and Carlos González
An Implementation of Blokus Duo player on FPGA Akira Kojima