The 2013 International Conference on Field-Programmable Technology

ICFPT 13

Kyoto Research Park, Kyoto, Japan, Dec. 9-11, 2013

ICFPT is the premier conference in the Asia-Pacific region on field-programmable technologies including reconfigurable computing devices and systems containing such components. Field-programmable devices promise the flexibility of software with the performance of hardware. The development and application of field-programmable technology have become important topics of research and development. Field-programmable technology is widely applied, in high-performance computing systems, embedded and low-power control instruments, mobile communications, rapid prototyping and product emulation, among other areas.

Submissions are solicited on new research results and detailed tutorial expositions related to FPT, including but not limited to:

- **Tools and Design techniques** for FPT including placement, routing, synthesis, verification, debugging, run-time support, technology mapping, partitioning, parallelization, timing optimization, design and run-time environments, languages and modeling techniques, provably-correct development, intellectual property core-based design, domain-specific development, hardware/software co-design.
- **Architectures** for FPT including field-programmable gate arrays, complex programmable logic devices, coarse-grained reconfigurable arrays, field-programmable interconnect, field-programmable analogue arrays, field-programmable arithmetic arrays, memory architectures, interface technologies, low-power techniques, adaptive devices, reconfigurable computing systems, high-performance reconfigurable systems, evolvable hardware and adaptive computing, fault tolerance and avoidance.
- **Device technology** for FPT including programmable memories such as non-volatile, dynamic and static memory cells and arrays, interconnect devices, circuits and switches, and emerging VLSI device technologies.
- **Applications** of FPT including biomedical and scientific computation accelerators, network processors, real-time systems, rapid prototyping, hardware emulation, digital signal processing, interactive multimedia, machine vision, computer graphics, cryptography, robotics, manufacturing systems, embedded applications, evolvable and biologically-inspired hardware, financial application, big data management, aerospace and extreme environment applications
- **Education** for FPT including courses, teaching and training experience, experiment equipment, design and applications.

Submission Guidelines

The program committee solicits papers describing original research or high quality tutorial expositions in field-programmable technology, including, but not limited to, the areas of interest indicated above. High quality posters are also solicited. Current postgraduate research students are invited to submit a short paper detailing their proposed research to be presented in a poster-based Ph.D. forum. Papers should be submitted electronically via the conference website in PDF format, following the IEEE style. Full papers should not exceed 8 pages in length, while posters should not exceed 4 pages in length. Ph.D. forum papers are limited to 2 pages. FPT2013 uses a blind reviewing system. Manuscripts must not identify authors or their affiliations. Self-reference should be blanked out. Papers that identify authors will NOT be considered. Proposal for half and full day tutorials in the areas of interest are also sought. Tutorials are likely to be scheduled for 8, 11 or 12 December.

Design Competition

Implement the good player of Blokus Duo – please refer to the design competition website for details; http://lut.eee.u-ryukyu.ac.jp/dc13/

Sponsorship

Enquiries regarding financial sponsorship should be directed to the Demo Session Chairs.

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Key Dates:
Early registration: Nov.1, 2013

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FORTH CALL FOR PAPERS

http://www.icfpt.org

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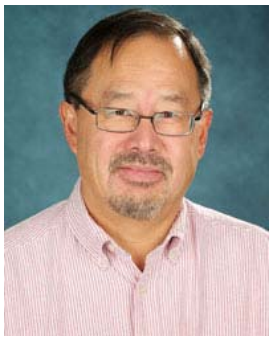
Keynote Presentations



Why Put FPGAs in Your CPU Socket?
Paul Chow (University of Toronto, Canada)
Abstract: Ever since FPGAs were invented, there has been great interest in using them as computing devices, and with the logic densities of today's devices, many interesting functions have been shown to have significant performance and energy benefits when implemented in FPGAs. However, when an application requires the combination of a high-performance CPU and an FPGA accelerator, the effectiveness of the FPGA is highly determined by the latency and bandwidth between the CPU, the CPU memory system and the FPGA and its memory system. Putting FPGAs into the CPU socket is one way to address this issue. This talk will present the history, the advantages and disadvantages, the challenges, architectures, programming models and applications of "in-socket" accelerator systems.

Recent Advances in Die Stacking and 3D FPGA
Arifur Rahman (Altera, USA)
Abstract: Die stacking technology with high-bandwidth interconnect is enabling new product architectures and capabilities. Although 3D integration, where TSVs are incorporated in active device layers, is the Holy-Grail of die stacking, the early phase of technology adoption is driven by passive silicon interposer (2.5D) based integration scheme or some variants of it. This presentation will provide an overview of recent advances in die stacking and FPGA application trends which are driving the need for stacking technologies. I will present some of the industry challenges in technology integration and design infrastructure and how they are being addressed to enable broader technology adoption.

Reconfigurable chip Advantage compared with GPGPU from the compiler perspective
Kazutoshi Wakabayashi (NEC Corporation)
Abstract: This presentation discusses how FPGA or coarse grained reconfigurable processor is superior to CPU/GPGPU from the view point of C compiler. Initially, we introduce the architectural characteristic of CPU, GPGPU and fine grained and coarse grained reconfigurable process with FSM+Datapath model. Then, we explain what kind of applications can be accelerated with "FPGA and C-based High Level Synthesis Tool" better than GPGPU according to the compiler techniques (freedom of compiler parallelization).

FPT2013 Program at a Glance

Dec.8 (Sun)	Dec.9 (Mon)	Dec.10 (Tue)	Dec.11 (Wed)	Dec.12 (Thu)	Dec.13 (Fri)
- Preliminary Design Comp.	- Opening - Keynote - Tech. Program - Reception	- Keynote - Tech. Program - Banquet	- Keynote - Tech. Program - Closing - Design Comp.	- Tutorial - Workshop	- Tutorial - Workshop

Contact Address

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Sponsor / Exhibition: ml-fpt13exh@ml.ritsumei.ac.jp
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