

CALL FOR PARTICIPATION

*The 5th International Symposium on
Highly-Efficient Accelerators and Reconfigurable Technologies*

HEART2014

Sendai, Japan [June 9 - June 11, 2014]

The 5th International Symposium on Highly Efficient Accelerators and Reconfigurable Technologies (HEART) is a forum to present and discuss new research on accelerators and the use of reconfigurable technologies for high-performance and/or power-efficient computation. Submissions are solicited on a wide variety of topics related to acceleration for high-performance computation, including but not limited to:

Architectures and systems:

- + Novel systems/platforms for efficient acceleration based on FPGAs, GPUs, and other devices
- + Heterogeneous processor architectures and systems for scalable, high-performance, high-reliability, and/or low-power computation
- + Reconfigurable and configurable hardware and systems including IP-cores, embedded systems, SoCs, and cluster/grid/cloud computing systems for scalable, high-performance and/or low-power processing
- + Custom computing systems for domain-specific applications such as Big-data, multimedia, bioinformatics, cryptography, and more
- + Novel architectures and device technologies that can be applied to efficient acceleration, including many-core/NoC architectures, 3D-stacking technologies and optical devices

Software and applications:

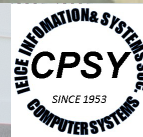
- + Novel applications of high-performance computing and Big-data processing with efficient acceleration and custom computing
- + System software, compilers and programming languages for efficient acceleration systems / platforms, including many-core processors, GPUs, FPGAs and other reconfigurable /custom processors
- + Run-time techniques for acceleration, including Just-in-Time compilation and dynamic partial-reconfiguration
- + Performance evaluation and analysis for efficient acceleration
- + High-level synthesis and design methodologies for heterogeneous, reconfigurable and/or custom processors/systems

FPGA Design Contest 2014 (Registration Due: May 7, 2014)

Following the FPGA design competition in ICFPT2013, we are planning another Blokus Duo design contest at HEART2014. The regulation of this contest is slightly different from that of ICFPT2013; the new regulation reduces the first-move advantage in the previous regulation. To get more information, please visit: <http://lut.eee.u-ryukyu.ac.jp/dc14/>.

Exhibition and Sponsorship Opportunities

Sponsorship is available to both exhibitors and non-exhibitors, with opportunities available to sponsor items, company logo display, sponsored sessions and breaks, dinner drinks reception, and prizes.



HEART2014 Keynote lectures (All of the detail is still to come.)

Prof.-Dr. Boku Taisuke, University of Tsukuba, Japan
Towards Reconfigurable High Performance Computing based on Co-Design Concept

Mr. Harold Noyes, Micron Technology, Inc.
Micron's Automata Processor Architecture:
Reconfigurable and Massively Parallel Automata Processing

NVIDIA
T.B.A.

HEART2014 Program Summary (All of the detail is still to come.)

June 8 (Sun)	June 9 (Mon)	June 10 (Tue)	June 11 (Wed)	June 12 (Thu)	June 13 (Fri)
Workshop/Tutorial	HEART2014	HEART2014	HEART2014	IEICE RECONF	IEICE RECONF
Workshop/Tutorial	HEART2014	HEART2014	HEART2014	IEICE RECONF	IEICE RECONF
N/A	HEART reception	HEART Banquet	Design Contest	IEICE Banquet	N/A

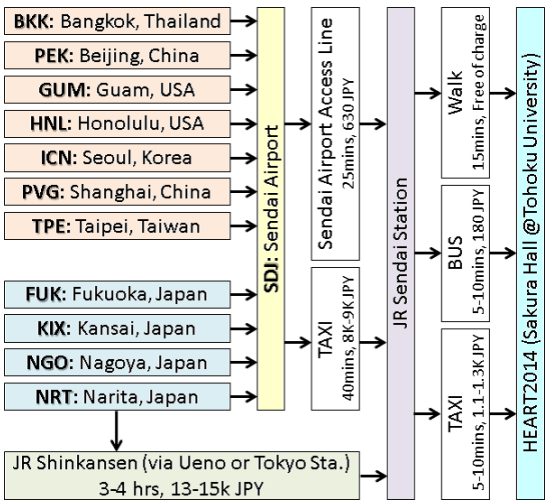
Organizing Committee

General Chair Hideharu Amano, Keio University, JP	Publicity Co-Chairs Miriam Leeson, Northeastern University, US David Thomas, Imperial College London, UK Yoshiki Yamaguchi, University of Tsukuba, JP	Publication Co-Chairs Yuichiro Shibata, Nagasaki University, JP Hironori Nakajo, Tokyo University of Agriculture and Technology, JP
Vice Co-Chairs Martin Herbordt, Boston University, US Kentaro Sano, Tohoku University, JP	Special-session Co-Chairs Masanori Hariyama, Tohoku University, JP (Big data) Michael Hubner, Karlsruhe Institute of Technology, DE (Dynamic Reconfig.) Hiroyuki Takizawa, Tohoku University, JP (HPC)	Industrial Co-Chairs Hiroaki Inoue, NEC Green Platform Research Labs, JP Khaled Benkrid, ARM, UK
Technical Program Co-Chairs Toshihiro Hanawa, University of Tokyo, JP Hayden Kwok-Hay So, University of Hong Kong, HK Lesley Shannon, Simon Fraser University, CA	Exhibition Chair Ryusuke Egawa, Tohoku University, JP	Local Arrangement Co-Chairs Hasitha Waidyasooriya, Tohoku University, JP Tomohiro Ueno, Tohoku University, JP
Finance Chair Yukinori Sato, JAIST, JP		Design Competition Chair Yasunori Osana, Univ of the Ryukyus, JP

Technical Program Committee (TBD)

Ali Akoglu, University of Arizona, US
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Zoltan Nagy, Hungarian Academy of Sciences, HU
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Tanya Vladimirova, University of Leicester, UK
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Yu Wang, Tsinghua University, CN
Minoru Watanabe, Shizuoka University, JP
Stephan Wong, Delft University of Technology, NL
Masato Yoshimi, Doshisha University, JP

Access



Sendai airport (SDJ) is about 20km from the centre of Sendai Miyagi, Japan. There are regular international flight services from Bangkok (BKK), Beijing (PEK), Guam (GUM), Honolulu (HNL), Seoul (ICN), Shanghai (PVG), and Taipei (TPE).

If other cities, you can arrive at SDJ by changing your flight at Japanese domestic airports: Narita (NRT), Kansai (KIX), Nagoya (NGO), Fukuoka (FUK), and so on.

From JR Sendai station to Katahira Sakura Hall

- Walk (15 min, about 1.5km)
- Bus (5-10min, 180 JPY)
- Taxi (5-10 min, 1100-1300 JPY)

From Sendai Airport (SDJ) to JR Sendai station

- Train (Sendai Airport Line: 25 min, 630 JPY)
- Taxi (40 min, 8,000-9,000 JPY)



JR Sendai station



Katahira Sakura Hall

Important Dates (23:59:59, GMT):

Early registration : **March 7, 2014**
D. Contest Due date: **March 7, 2014**
Symposium dates : **June 9 to 11, 2014**
Design Contest date : **June 11, 2014**

