HEART2014 Fifth International Symposium on Highly-Efficient Accelerators and Reconfigurable Technologies

HEART2014 Advanced Program

Day 1 : June 9	
08:40-17:30	Registration
09:00-09:10	Opening
09:10-10:10	**Keynote Session 1** Session chair: Hideharu Amano (Keio University)
	Towards Reconfigurable High Performance Computing based on Co-Design Concept Prof. Taisuke Boku, University of Tsukuba
10:10-11:10	Coffee break & exhibition
11:10-12:25	**Session 1: Multi-GPU Systems & Applications** Session chair: Yuichiro Shibata (Nagasaki University)
	PEACH2: FPGA based PCIe network device for Tightly Coupled Accelerators Yuetsu Kodama, Toshihiro Hanawa, Taisuke Boku and Mitsuhisa Sato
	Performance analysis of the multi-GPU System with ExpEther Shimpei Nomura, Takuji Mitsuishi, Jun Suzuki, Yuki Hayashi, Masaki Kan and Hideharu Amano
	GPU acclerated Hybrid Tree Algorithm for Collision-less N-body Simulations Tsuyoshi Watanabe and Naohito Nakasato
12:25-14:00	Lunch
14:00-15:15	**Session 2: Image Processing** Session chair: Yoshiki Yamaguchi (University of Tsukuba)
	GPU and FPGA Acceleration of Level Set Method Haruhisa Tsuyama and Tsutomu Maruyama
	Fast and Accurate Optical Flow Estimation using FPGA Yu Tanabe and Tsutomu Maruyama
	Area-time efficient implementation of local adaptive image thresholding in reconfigurable hardware Cesar Torres-Huitzil and Marco Aurelio Nuno Maganda
15:15-16:00	Coffee break & exhibition
16:00-17:15	**Special Session: High Performance Reconfigurable Computers** Session chair: Lesley Shannon (Simon Fraser University)
	Reconfigurable Multiprocessor Systems: Handling Hydras Heads – A Survey Diana Gohringer
	FPGA-based Custom Computing Architecture for Large-Scale Fluid Simulation with Building Cube Method Kentaro Sano, Ryotaro Chiba, Tomoya Ueno, Hayato Suzuki, Ryo Ito and Satoru Yamamoto
	GRT: a Reconfigurable SDR Platform with High Performance and Usability Tao Wang, Guangyu Sun, Jiahua Chen, Jian Gong, Haoyang Wu, Xiaoguang Li, Songwu Lu and Jason Cong
17:15-17:30	Coffee break & exhibition
17:30-19:30	Reception

Day 2 : June 10

08:40-12:30	Registration
09:00-10:00	**Keynote Session 2** Session chair: Kentaro Sano (Tohoku University)
	Micron's Automata Processor Architecture: Reconfigurable and Massively Parallel Automata Processing Mr. Harold Noyes, Micron Technology
10:00-10:10	**Sponsor Talk** Session chair: Ryusuke Egawa (Tohoku University)
	Keio University [link]
10:10-11:10	**Poster Session 1** Session chair: Hasitha Waidyasooriya (Tohoku University)
11:10-12:25	**Session 4: Design Methodology** Session chair: Yukinori Sato (JAIST)
	A case study of FPGA Blokus Duo Solver by System-Level Design Yuki Ando, Masataka Ogawa, Yuya Mizoguchi, Kouta Kumagai, Miaw Torng-Der and Shinya Honda
	Searching for sinks of Henon map using a multiple-precision GPU arithmetic library Mioara Joldes, Valentina Popescu and Warwick Tucker
	A Memory Profiling Framework for Stencil Computation on an FPGA Accelerator with High Level Synthesis Rie Soejima, Koji Okina, Keisuke Dohi, Yuichiro Shibata and Kiyoshi Oguri
12:25-13:30	Lunch
13:30-18:00	Short tour
18:00-20:00	Banquet

Day 3 : June 11

08:40-12:30	Registration
09:00-10:00	**Keynote Session 3** Session chair: Hiroyuki Takizawa (Tohoku University)
	Towards a Scalable and Configurable Accelerator Dr. Simon See, NVidia Inc.
10:00-11:00	**Poster Session 2** Session chair: Hasitha Waidyasooriya (Tohoku University)
11:00-12:15	**Session 5: Graph Processing & Low Energy Systems** Session chair: Toshihiro Hanawa (University of Tokyo)
	Performance Evaluations of Graph Database using CUDA and OpenMP-Compatible Libraries Shin Morishima and Hiroki Matsutani
	Accelerating Breadth First Search on GPU-BOX Takuji Mitsuishi, Shimpei Nomura, Jun Suzuki, Yuki Hayashi, Masaki Kan and Hideharu Amano
	Energy efficient Reconfigurable Computing with Adaptive Voltage and Logic scaling Jose Nunez-Yanez
12:15-12:30	Closing
12:30-13:30	Lunch
13:30-16:50	FPGA Design Contest
16:50-17:00	Break
17:00-17:50	Invited speech by IEICE RECONF Workshop (in Japanese)
18:00-20:00	Reception of IEICE RECONF Workshop (in Japanese)

Posters	
June 10 10:10-11:10	***Parallelization of Booth's Multiplications on a Multi-ALU Processor*** Lin Meng, Daichi Kinekawa, Haruaki Ishikawa and Katsuhiro Yamazaki
	Efficient shared cache system for ARM-based multi-core processors Hongkun Jin, Yoshiki Yamaguchi and Yuetsu Kodama
	Leakage Reduction using Coarse-Grained Static Body Biasing in a Dynamically Reconfigurable Processor Johannes Maximilian Kühn, Hideharu Amano, Toru Katagiri and Wolfgang Rosenstiel
	Design Partitioning Optimization and Context Storages Selection for Cost Efficient FPGA Application with Partial Reconfiguration Technologies Kar Foo Chong, Kentaro Sano and Bee Ling Tan
	An Asynchronous High-Performance FPGA Based on LEDR/Four-Phase-Dual-Rail Hybrid Architecture Yoshiya Komatsu, Masanori Hariyama and Michitaka Kameyama
June 11 10:00-11:00	***An AWF Spectrometer On a Radio Telescope*** Hiroki Nakahara, Hiroyuki Nakanishi, Kazumasa Iwai and Tsutomu Sasao
	A Reconfigurable Vector Instruction Processor for Accelerating a Convection Parametrization Model on FPGAs Syed Waqar Nabi, Saji N. Hameed and Wim Vanderbauwhede
	A parallel-operation-oriented FPGA architecture Minoru Watanabe
	FPGA-Accelerator for DNA Sequence Alignment Based on an Efficient Data-Dependent Memory Access Scheme Hasitha Waidyasooriya, Masanori Hariyama and Michitaka Kameyama
	Programmable Protocol Processing Engine in Heterogeneous MP-SoC: A Case Study Mohammad Badawi, Huisheng Zhou, Zhonghai Lu and Ahmed Hemani