HEART 2013

Fourth International Symposium on Highly Efficient Accelerators and Reconfigurable Technologies

Edinburgh, Scotland
13-14 June 2013

Day 1 Thu 13th June

Time	Program
08:50 - 09:00	**Opening**
09:00 - 10:00	**Keynote lecture 1** Highly Efficient Designs: Art, Magic or Engineering? *by Ken Chapman*
10:00 - 10:30	**Coffee/Tea Break**
10:30 - 12:10	**Session 1: Best paper candidates** (1) Accelerating Sequential Monte Carlo Method for Real-time Air Traffic Management *Thomas C.P. Chau, James Stanley Targett, Marlon Wijeyasinghe, Wayne Luk, Peter Y.K. Cheung, Benjamin Cope, Alison Eele and Jan Maciejowski* (2) NCBI BLASTP on the Convey HC1EX *Atabak Mahram and Martin Herbordt* (3) Efficient Custom Computing of Fully-Streamed Lattice Boltzmann Method on Tightly-Coupled FPGA Cluster *Kentaro Sano, Yoshiaki Kono, Hayato Suzuki, Ryotaro Chiba, Ryo Ito, Tomohiro Ueno, Kyo Koizumi and Satoru Yamamoto* (4) A Hybrid CPU-FPGA System for High Throughput (10Gb/s) Streaming Document Classification *Wim Vanderbauwhede, Anton Frolov, Sai Rahul Chalamalasetti and Martin Margala*
12:10 - 14:00	**Session 2: Solarflare Luncheon Session** In this session, Solarflare will give a presentation on their University Program, followed by Q&A and one-to-one discussions. SOLARFLARE®
14:00 - 14:50	**Session 3: Applications** (5) Customisable Pipelined Engine for Intensity Evaluation in Multivariate Hawkes Point Processes *Ce Guo, Wayne Luk, Ekaterina Vinkovskaya and Rama Cont* (6) Accelerating Finite Difference Time Domain Simulations with Reconfigurable Dataflow Computers *Heiner Giefers, Christian Plessl and Jens Förstner*

14:50 - 16:20	**Session 4: Poster Presentation (Each poster paper has a 5-minute short presentation.)** (P1) Deadlock-Free Routing Strategy for Stacking 3-D NoCs with Different Topologies *Daisuke Sasaki, Hiroki Matsutani, Michihiro Koibuchi and Hideharu Amano* (P2) An Energy Effective SIMD Accelerator for Visual Pattern Matching *Calin Bira, Liviu Gugu, Radu Hobincu, Valeriu Codreanu, Lucian Petrica and Sorin Cotofana* (P3) A 7-depth search FPGA Connect6 Solver *Retsu Moriwaki, Takashi Yoza, Yuki Kamikubo, Yuki Torigai, Akira Tanigawa, Takayuki Kubota, Hiroyuki Ito, Yuya Shirahashi and Minoru Watanabe* (P4) High Performance Gapped BLAST with the Two-hit Method Implementation on FPGA *Mohd Nazrin Md Isa, Khaled Benkrid and Thomas Clayton* (P5) Cache-aware Parallel Programming for Manycore Processors *Ashkan Tousimojarad and Wim Vanderbauwhede* (P6) Intensity and Distance Thresholding in Hardware to Enable Flexible Blob Detection for a Vision System with Limited Bandwidth *Peter Samarin, Timur Saitov, Rainer Herpers and Kenneth Kent*
16:20 - 17:10	**Session 5: High-level-language reconfigurable systems** (7) A reconfigurable Java accelerator with software compatibility for embedded systems *Yuki Ogawa, Masahiro Iida, Motoki Amagasaki, Morihiro Kuga and Toshinori Sueyoshi* (8) Reconfigurable and Hardwired ORB Engine by Java-to-HDL Synthesizer for Realtime Application *Takeshi Ohkawa, Daichi Uetake, Takashi Yokota, Kanemitsu Ootsu and Takanobu Baba*
19:00-22:30	**Banquet at City Chambers (253 High Street, Edinburgh, EH1 1YJ)** City Chambers is a fantastic historic building founded in 1761 and now used as the home of the City of Edinburgh Council, in Scotland. All registered attendees are welcome to join this banquet; costs have been included in the registration fee.

Day 2 Fri 14th June

Time	Program
09:00 - 10:00	**Keynote lecture 2** Execution time should be as short as possible, but not shorter *by Dr. David Broman*
10:00 - 11:30	**Session 6: Poster Presentation (Each poster paper has a 5-minute short presentation.)** (P7) Granularity Problem of Runtime Reconfigurable Design Flows *Dominik Meyer and Bernd Klauer* (P8) A Fast Runtime Visualization Framework for Efficient Development of Scientific Applications on CUDA *Kota Aoki, Keisuke Dohi, Yuichiro Shibata and Kiyoshi Oguri* (P9) High Accuracy Low Memory Logarithmic Converter *Syed Ahmed, Srinivas M.B, Pavan Sastry and Sreehari V. A* (P10) CMASOTB/LPT-3: The first prototype chip of Cool Mega Array on Silicon On Thin BOX *Hongliang Su, Weihan Wang, Kuniaki Kitamori and Hideharu Amano* (P11) A dependability-increasing demonstration for a 16-configuration context optically reconfigurable gate array *Akira Tanigawa and Minoru Watanabe* (P12) Chebyshev Polynomial Smoother in Multiple GPU-based AMG Method *Yuki Araya, Akihiro Fujii and Teruo Tanaka*
11:30 - 12:20	**Session 7: Numeric operation** (9) Fixed-Point Trigonometric Functions on FPGAs *Florent De Dinechin, Matei Istoan and Guillaume Sergent* (10) Performance Evaluation of 3-D Stacked 32-bit Parallel Multipliers *Jubee Tada*

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12:20 - 14:00	**Lunch Break**
14:00 - 14:50	**Session 8: Architecture** (11) The Ultrasmall Soft Processor *Yuichiro Tanaka, Shimpei Sato and Kenji Kise* (12) Customisable Architectures for the Set Covering Problem *Liucheng Guo, David Thomas and Wayne Luk*
14:50 - 15:20	**Coffee/Tea Break**
15:20 - 16:10	**Session 9: Reconfigurable SoCs** (13) Blueshell: A Platform for Rapid Prototyping of Multiprocessor NoCs and Accelerators *Gary Plumbridge, Jack Whitham and Neil Audsley* (14) A Run-time Reconfigurable System for Adaptive High Performance Efficient Computing *Chuan Hong, Khaled Benkrid, Nazrin Isa and Xabier Iturbe*
16:10 - 16:40	**Closing & Award Ceremony**

Notes:
- Each regular paper has a 20-minutes full-time speech and a 5-minute discussion.
- Each poster paper has a 5-minute short-time speech and 1-hour poster presentation.
- The best paper award will be judged by HEART2013 Program Committee in the session of the best paper candidates.
- The best poster award will be selected from all poster presentations.
- HEART2013 award ceremony will be held in the closing talk.
- The no-show regular paper will not be invited to the post proceedings published by ACM CAN.
- The size of the poster could be as large as A0 (1189 x 841 mm), portrait orientation.