Internatioal Workshop on Highly-Efficient Accelerators and Reconfigurable Technologies

Okinawa, **Japan** [May 31 - June 1, 2012]

CALL FOR PAPERS

The 3rd International Workshop on Highly Efficient Accelerators and Reconfigurable Technologies (HEART) is a forum to present and discuss new research on accelerators and the use of reconfigurable technologies for high-performance and/or power-efficient computation. Submissions are solicited on a wide variety of topics related to the acceleration for high-performance computation, including but not limited to:

Architectures and systems:

- Novel systems/platforms for efficient acceleration based on FPGA, GPU, CELL/B.E and other devices
- Heterogeneous processors/systems for scalable, high-performance, high-reliability and/or low-power computation
- Reconfigurable/configurable hardware and systems including IP-cores, embedded systems, SoCs and cluster/grid/cloud computing systems for scalable, high-performance and/or low-power processing
- High-performance custom-computing processors and systems
- Novel architectures and device technologies that can be applied to efficient acceleration, including many-core architectures, NoC architectures, 3D-stacking technologies and optical devices

Software and applications:

- Novel applications for efficient acceleration systems/platforms, and custom computing
- Compiler techniques and programming languages for efficient acceleration systems/platforms, including many-core processors, GPUs, FPGAs and other reconfigurable/custom processors
- Run-time techniques for acceleration, including Just-in-Time compilation and dynamic partial-reconfiguration
- Performance evaluation and analysis for efficient acceleration
- High-level synthesis and design methodologies for heterogeneous, reconfigurable and/or custom processors/systems

We will accept regular and short papers for oral and poster presentation, respectively. All the accepted regular papers will be published in the post-proceedings that will be published as a special issue of ACM SIGARCH Computer Architecture News and will also be available in ACM Digital Library. Papers are limited to 6 pages (two columns, US letter size, 10 points for main body text), and must be prepared in PDF format. Paper submission is now open at http://www.isheart.org/HEART2012/.



Keynote lecture:

Tsuyoshi Hamada, Ph.D Gordon Bell prize for price/performance at SC'09 DEGIMA:

The greenest accelerator-based supercomputer in TOP500 list

IMPORTANT DATE:

- Submission deadline: Feb. 21, 2012
- Acceptance notification: Mar. 26, 2012
- Camera-ready deadline: Apr. 12, 2012
- Workshop date : May 31 Jun. 1, 2012





Organizing Committee:

Workshop Co-Chairs

Hideharu Amano (Keio University, JP) Wayne Luk (Imperial College London, UK)

Program Co-chairs:

Yukinori Sato (JAIST, JP)
Walid Najjar (University of California Riverside, USA)
David Thomas (Imperial College London, UK)

Finance chair:

Kentaro Sano (Tohoku University, JP)

Publication Co-chairs:

Yuichiro Shibata (Nagasaki University, JP)
Hironori Nakajo (Tokyo University of Agriculture and Technology, JP)

Publicity Co-chairs:

Khaled Benkrid (the University of Edinburgh, UK)

Qiang Liu (Tianjin University, CN)

Yoshiki Yamaguchi (University of Tsukuba, JP)

Local Arrangement Chair:

Yasunori Osana (University of the Ryukyus, JP)

Design Contest Co-chairs:

Tomonori Izumi (Ritsumeikan University, JP)
Minoru Watanabe (Shizuoka University, JP)

http://www.isheart.org/



30 May, 2012 Okinawa Japan

This contest will be held in conjunction with HEART2012 http://www.isheart.org