HEART2010

Internatioal Workshop on Highly-Efficient Accelerators and Reconfigurable Technologies

CALL FOR PAPERS

The 1st international workshop on Highly Efficient Accelerators and Reconfigurable Technologies (HEART) is a forum to present and discuss new research on accelerators based on reconfigurable technologies for high-performance and/or power-efficient computation. Submissions are solicited on a wide variety of topics related to high-performance reconfigurable computation and other accelerators including GPGPUs and Cell/B.E, including but not limited to:

Important dates (JST, UTC+9) :

Paper submission: April 17th
Author notification: April 28th
Acceptance notification: May 3rd
Workshop date: June 1st

Conference place :

Epocal Tsukuba, Tsukuba, Ibaraki, Japan

Architectures and systems:

o Reconfigurable/configurable hardware and systems including IP-cores, embedded systems and/or SoCs for scalable, high-performance and/or low-power computation
o High-performance custom-computing systems based on reconfigurable technologies including FPGAs
o Grid/cluster computing with FPGAs, other reconfigurable technologies and accelerators such as GPGPUs and Cell/B.E.s
o Novel architectures and devices that can be applied to efficient acceleration, including many-core architectures, NoC architectures, and optical devices/interconnection

Software and applications:

o Novel applications for high-performance reconfigurable systems and other accelerators including GPGPUs and Cell/B.E.
o Compiler techniques and programming languages for reconfigurable acceleration systems and other accelerators such as GPGPUs and Cell/B.E.
o Run-time systems and the use of run-time reconfigurability for acceleration
o Performance evaluation and analysis of reconfigurable acceleration systems and other accelerators such as GPGPUs and Cell/B.E.

Co-sponsorship :

EiC The Institute of Electronics, Information and Communication Engineers
Technical Committee on Reconfigurable Systems

Workshop committees :

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